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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/789,883	02/27/2004	Alon Saado	2650.00016	9328

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EXAMINER

TU, CHRISTINE TRINH LE

ART UNIT PAPER NUMBER

2138

DATE MAILED: 11/27/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

## Office Action Summary

Application No.

10/789,883

Applicant(s)

SAADO ET AL.

Examiner

Christine T. Tu

Art Unit

2138

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 29 September 2006.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1-14 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-8, 10-12 and 14 is/are rejected.
- 7) ☒ Claim(s) 9 and 13 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
  - ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- |  |   |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)   | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                       | 5) <input type="checkbox"/> Notice of Informal Patent Application                       |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

***Claim Rejections - 35 USC § 103***

1. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

2. Claims 1-8, 10-12 and 14 are again rejected under 35 U.S.C. 103(a) as being unpatentable over Allen (5,878,055).

**Claims 1-3:**

Allen discloses the invention substantially as claimed. Allen shows that a single phase clock verification apparatus (200) includes a plurality of variable delay clock blocks (202) respectively coupled to a plurality of latches (204). The plurality of latches (204) include a variable delay clock block T1, (210) for providing at its output a clock signal CLOCK1, a variable delay clock block T2, (212) for providing at its output a clock signal CLOCK2, a variable delay clock block T3, (214) for providing at its output a clock signal CLOCK3, and a variable delay clock block T4, (216) for providing at its output a clock signal CLOCK4. During a scan operational mode, the delays of all the variable delay blocks (202) are set to the same value between latches (204) in the scan chains. During the test operational mode, the delay through the delay clock blocks (202) depends upon the settings in the delay control register (220), so the clock going to the various latches is delayed various amounts (figures 2 & 5, column 3 lines 30-44, column 4 lines 33-37, column 6 lines 25-67).

Allen does not explicitly teach the logic elements. Sullivan, however, teaches each Boundary scan cell (BSC) (52) comprises a comparator circuit (60) (figure 5).

It would have been obvious to one skilled in the art at the time the invention was made to realize that Allen's each of the latches (204) would be comprised of a comparator/XOR (logic) circuit (as suggested by Sullivan). One having ordinary skill in the art would be motivated to realize so because both Allen and Sullivan teach the sequential latches or boundary scan cells (BSCs).

Claim 4:

In the scan mode, Allen teaches that all of the variable delay clock blocks (202) have the same delay. As the clock (CLK) toggles, the applied data depends on the setting of the bits in the delay control register (220). The delay control register (22) is programmed with the combination of states that selects the desired amount of clock delay for each variable delay clock blocks (202) (column 6 lines 45-59).

Claim 5:

In the test mode, Allen teaches that the delay through the delay clock blocks (202) depends upon the plurality settings in the delay control register (220), so the clock going to the various latches is delayed various amounts (plural) (column 6 lines 60-67).

Claim 6:

Allen's latches (204) can be flip-flops (column 3 line 66-67).

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Claim 7:

Allen teaches that the apparatus (200) allows to verify characterization of latch behavior with respect to early mode failures so that the early mode problems can be corrected, wherein early mode is known as latch hold time violation (column 3 lines 45-55, column 2 lines 1-5, column 1 lines 21-22).

Claim 8:

Allen teaches the scan mode is used to initialize the circuit (200), then the test mode is used, and later the scan mode is also used to observe the results of operations of the previous test operational mode (column 6 lines 39-44).

Claims 10-12 and 14:

Claims (10 & 14), 11 and 12 are rejected for reasons similar to those set forth against claims 1, 8 and 7 respectively.

***Response to Arguments***

3. Applicant's arguments filed September 29, 2006 have been fully considered but they are not persuasive.

Applicant argues that Allen fails to disclose the limitation of the shift mode operates with multiple scan clocks that are toggled simultaneously. Examiner, however, disagrees against applicant's remark. Such feature is taught by Allen. Allen teaches that during the scan mode, the delays of all the variable delay blocks (202) are set to

the same value to prevent early mode between latches (204) in the scan chains (column 6 lines 25-29). In other words, all of the CLOCK1, CLOCK2, CLOCK3 and CLOCK4 are synchronized/toggled simultaneously by setting the same value during the scan/shift mode.

Applicant also alleges that Allen fails to teach the presently claimed capture mode which operates within multiple scan clocks with only one of the scan clock being toggled at a time. Allen, however, does teach such feature as well. Allen teaches that in the test mode, the delay through the delay clock blocks (202) depends upon the settings in the delay control register (220), so the clock going to the various latches is delayed various amounts (column 6 lines 60-67). In other words, each of the latches is clocked by a (different) delayed clock. That means, each of CLOCK1, CLOCK2, CLOCK3 and CLOCK4 will be toggled in vary amount of time (not at the time).

4. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christine T. Tu whose telephone number is (571)272-3831. The examiner can normally be reached on Mon-Thur. 8:30am-6:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady can be reached on (571)272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

  
Christine T. Tu  
Primary Examiner  
Art Unit 2138

November 21, 2006